IDEC Chip Design Contest

Design of Dynamic Vision Sensors with Common-Gate Photoreceptor structure

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INTRODUCTION

Dynamic vision sensor (DVS) is a neuromorphic event-driven sensor which transforms temporal contrast (TC) of light intensity of a pixel into spike event. Event and x-y address data of the pixel are transmitted through asynchronous address event representation (AER) digital circuits. As DVS operates in the event-driven manner, the representation of the data is inherently sparse and no data redundancy exists. These properties are a great advantage in real time simulation compared to conventional image sensors.

Important performance specifications of DVS are pixel noise and TC sensitivity. Higher TC sensitivity leads to finer expression of texture. In [1], preamplifier stage is added before capacitive differencing amplifier stage for pixel gain enhancement. High TC sensitivity was obtained with a trade-off of pixel dynamic range. In [2], replaced the common-source differencing amplifier with pseudo-cascode two-stage Opamp, obtaining low noise performance and wide output range.

In this report, we tried to improve TC sensitivity using high density metal-insulator-metal(MIM) capacitor in SS65 process while limiting the noise level with common-gate photoreceptor (CGPR) structure.

CGPR photoreceptor design for DVS

Fig. 1 shows two types of photoreceptors used in DVSs. First one on the left is named as source-follower photoreceptor (SFPR). nFET on the feedback loop of the amplifier forms a source follower with the photodiode. The other one on the right is named as common-gate photoreceptor (CGPR) because of the common-gate pFET feedback loop. It is widely known that pFETs tend to have a lower 1/f noise compared to nFETs. As low noise level is essential for high TC sensitivity circuit design, CGPR is more likely to be chosen for the high performance DVS implementation.

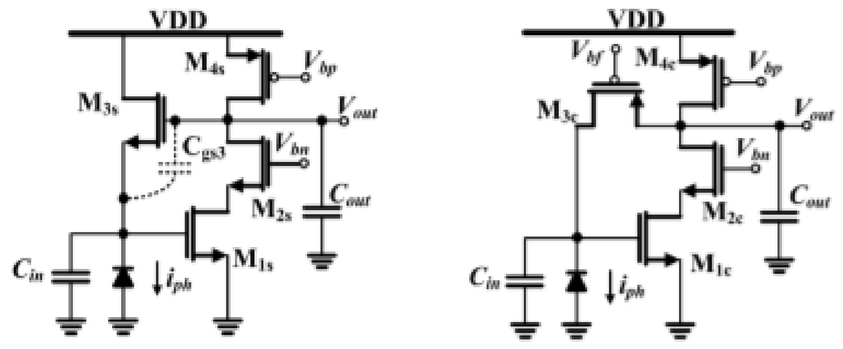

Fig.1. Schematic diagrams of two different circuits
(a) Source-follower Photoreceptor, (b) Common-gate Photoreceptor

For improving the signal swing range, this works used the Low threshold voltage transistors (LVT Tr.). The V_{GS} of the Tr.$_{CG}$ in the fig. 1. is directly function of the threshold voltage. If the lower threshold voltage is used, the lower cut-off voltage is introduced as shown in the fig. 3. Therefore, the feedback loop is extend to lowest signal range because the feedback loop can be operated by the reduced threshold voltage.

Cadence Spectre noise simulation for the CGPR architecture are simulated and plotted in Fig. 4. The simulation was done for photocurrent I_{ph} from $10fA$ to $10nA$ with different integration bandwidths from 100Hz to 10MHz. As shown in the result, plateaus exist in each different bandwidth. Cadence Spectre noise simulation for the CGPR architecture are simulated and plotted in Fig. 4. Cadence Spectre noise simulation for the CGPR architecture are simulated and plotted in Fig. 4. The simulation was done for photocurrent I_{ph} from $10fA$ to $10nA$ with different integration bandwidths from 100-Hz to 10MHz. As shown in the result, plateaus exist in each different bandwidth. The wider bandwidth of the TIA the more noise power that is not filtered by extended pass band-width. It clearly shows that when the bandwidth of the photoreceptor is increased by increasing the photocurrent, the circuit is proportionally noisy. Thus, the bandwidth of the photoreceptor at some photocurrent can be inferred from the graph. For instance, The bandwidth of the one is 100Hz at $100fA$ while it widens to about 100kHz at $100pA$.

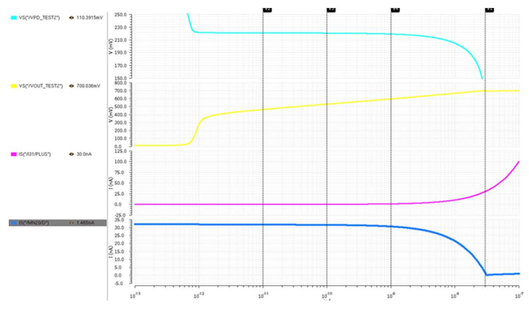

Fig.2. Enlarged signal range using low threshold voltage transistors

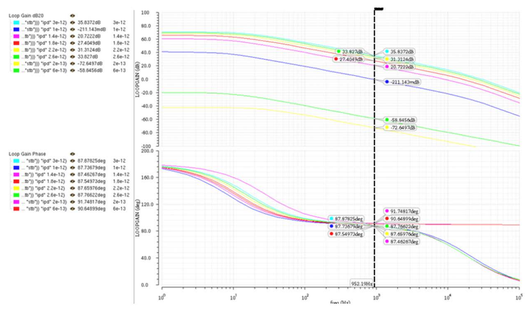

Fig.3. Current optimization for stability of the T.I.A

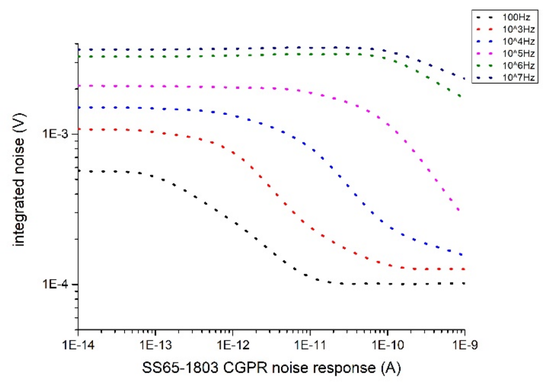

Fig. 4. SS65 Spectre-simulated output noise of CGPR with different pixel bandwidths

Measurement and Result

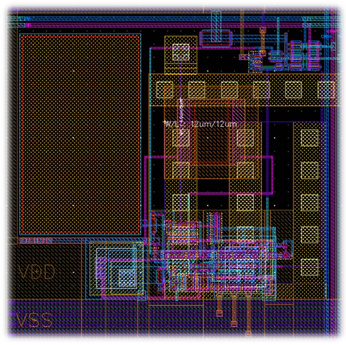

Fig.5. 25um x 25um DVS Pixel layout in 65nm process

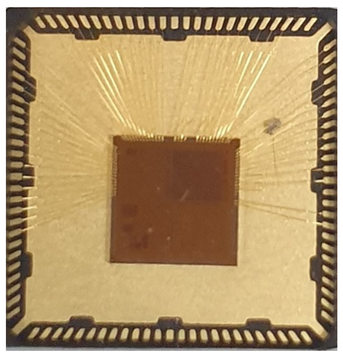

Fig.6. Chip microphotograph with QFN-100 package

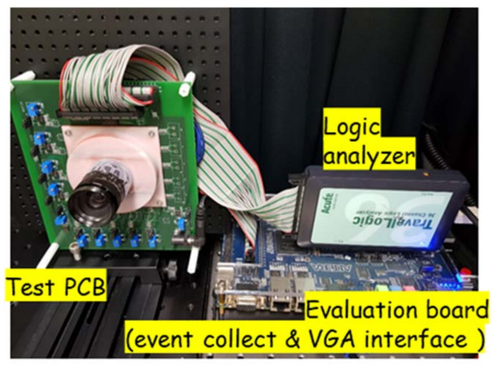

Fig.7. Test device and set-up enviroment

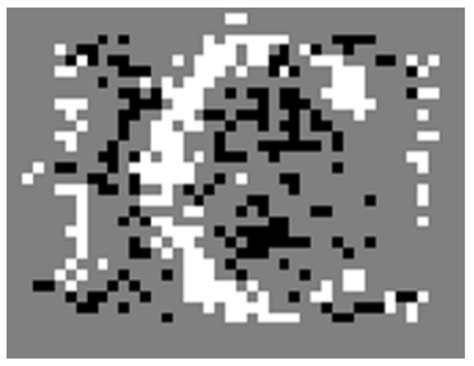

Fig.8. The captured Moving alphabet image

SS 1902 achieves less noise than the SFPR architecture of the DVS. This sensor generate much more output event data which is not noise but event. Therefore this chip of the CGPR architecture is less sensitive to noise and the image quality is improved.

ACKNOWLEDGEMENT
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